REMARKS

I. Summary of the Examiner's Action

A. Claim Rejections

In paragraph 2 of the Office Action, the Examiner rejected claims 1, 5 and 8 under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,532,632 to Kent (hereinafter "the Kent patent").

In paragraph 3 of the Office Action, the Examiner rejected claims 1, 5 and 8 under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,425,017 to Copley *et al.* (hereinafter "the Copley patent").

In paragraph 5 of the Office Action, the Examiner rejected claims 2 and 6 under 35 U.S.C. § 103(a) as being unpatentable over the Kent patent and further in view of Lee *et al.* in "Low-Noise Fast-Lock Phase-Locked Loop With Adaptive Bandwidth Control", IEEE Journal of Solid-State Circuits, vol. 35, no. 8, August 2000 (hereinafter "the Lee IEEE reference").

In paragraph 6 of the Office Action, the Examiner rejected claims 3 and 7 under 35 U.S.C. § 103(a) as being unpatentable over the Kent patent, and further in view of United States Patent Application No. 2003/0013412 A1 to Kardach *et al.*, (hereinafter "the Kardach application").

In paragraph 7 of the Office Action, the Examiner rejected claims 2 and 6 under 35 U.S.C. § 103(a) as being unpatentable over the Copley patent and further in view of the Lee IEEE reference.

In paragraph 8 of the Office Action, the Examiner rejected claims 3 and 7 under 35 U.S.C. § 103(a) as being unpatentable over the Copley patent in view of the Kardach application.

These rejections are respectfully disagreed with, and are traversed below.

B. Claim Objections and Allowable Subject Matter

In paragraph 9 of the Office Action the Examiner objected to claim 4 as being dependent upon a rejected base claim, but indicated that it would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

II. Applicant's Response – Claim Rejections

A. Rejection of Claims 1, 5 and 8 under 35 U.S.C. § 102(b) as being unpatentable over the Kent Patent

Claim 1 recites the following subject matter (emphasis added):

> 1. A circuit for controlling the duty cycle and jitter of a clock signal, comprising:
>
> an input node for receiving the clock signal; and

> an output node for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle.

Applicant has carefully examined the Kent patent and has not located the foregoing underlined subject matter. Instead Kent recites:

> Referring now to the drawings and initially to FIG. 1, the synchronizing circuit of the present invention is generally designated 10 and comprises an input terminal 12 for connection with a source of data D and an output terminal 14 providing an output data stream. A clock input terminal 16 is to be connected with a clock source CLK of predetermined frequency. The circuit 10 includes a variable or vernier time delay element 18 connected with the input terminal 12 for delaying the input data stream applied thereto. The element 18 provides an adjustable or programmable delay function, thereby producing at its Q output a data stream having transitions which are adjustable in time relative to the input data stream at its D input.

Column 2, lines 19 – 32 (emphasis added). Applicant respectfully submits that the most pertinent portion of the Kent reference neither describes nor suggests "an output node for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle" as recited in the underlined portion of claim 1 above. Rather, the apparatus of the Kent patent "outputs a data stream having transitions which

are adjustable in time relative to the input data stream at its D input." Kent apparently concerns correcting the timing of a data sequence, and has nothing to do with the subject matter of Applicant's invention. Applicant therefore respectfully requests that the Examiner withdraw the rejection of claim 1.

Applicant also respectfully requests that the Examiner withdraw the rejection of claims 5 and 8 for reasons similar to those set forth with respect to claim 1.

B. Rejection of Claims 1, 5 and 8 under 35 U.S.C. § 102(b) as being unpatentable over the Copley Patent

Applicant has carefully reviewed the portion of the Copley patent cited by the Examiner (column 4, line 40 – column 5, line 20) and does not understand how this relates to Applicant's invention. Applicant respectfully requests that the Examiner apply the Copley reference on an element-by-element basis so the Applicant can understand how the reference is being applied by the Examiner.

In addition, the Applicant understands that the Examiner purportedly finds "an output node for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle" as recited in claim 1 in the subject matter of the Copley patent corresponding to reference character 500. Applicant respectfully notes that reference character 500 does not refer to an output node as in the case of the Applicant's invention as recited in claim 1, but rather to "a phase jitter

analyzer circuit 500 for use in analyzing the results of the phase jitter test." Applicant reminds the Examiner that an anticipation rejection is a strict standard and that each and every element of the claim must be found in the relied-upon reference. Since the subject matter corresponding to reference character 500 of the Copley patent has nothing to do with an "output node . . ." as recited in claim 1, the Applicant respectfully requests that the Examiner withdraw the rejection of claim 1 on this basis alone.

Applicant also requests that the Examiner withdraw the rejection of claims 5 and 8 for reasons similar to those set forth with respect to claim 1.

C. Rejection of Claims 2 and 6 under 35 U.S.C. § 103(a) as being unpatentable over the Kent Patent in view of the Lee IEEE Reference

Applicant respectfully submits that claims 2 and 6, which respectively depend from claims 1 and 5, are patentable for the same reasons as set forth herein with respect to claims 1 and 5.

In addition, Applicant respectfully submits that the combination of the Kent patent and the Lee IEEE reference neither describes nor suggests "a circuit for controlling the duty cycle and jitter of a clock signal, comprising: an input node for receiving the clock signal; and an output node for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle" where the "predetermined duty cycle is a nominally 50-50 duty cycle" as recited in claim 2.

For these reasons, Applicant respectfully submits that claim 2 is patentable, and therefore requests that the rejection be withdrawn. Applicant also submits that claim 6 is patentable for similar reasons, and requests that the rejection of claim 6 be likewise withdrawn.

D. Rejection of Claims 3 and 7 under 35 U.S.C. § 103(a) as being unpatentable over the Kent Patent in view of the Kardach Application

Applicant respectfully submits that claims 3 and 7, which respectively depend from claims 1 and 5, are patentable for the same reasons as set forth herein with respect to claims 1 and 5.

In addition, Applicant has carefully read the portion of the Kardach application cited by the Examiner in combination with the Kent patent and does not see where there is a disclosure of an output node, as recited in claim 1 which "is coupled to baseband circuitry of a wireless communications terminal" as further recited in claim 3. For example, Applicant reproduces one of the portions of the Kardach application relied upon by the Examiner here:

> For example, consider the computer system of FIG. 1a comprising processor 305, memory 315, and input-output (1-0) device 320 coupled to bus control logic 310 (which is typically the system chipset). Short range wireless baseband controller 330 contains the logic associated with the full baseband, e.g. the Bluetooth baseband, used to operate transceiver 335. In other words, baseband controller contains all the logic used to support the full baseband of a wireless communications protocol. In addition,

> controller 330 contains bus interface logic used to communicate with bus control logic 310 of the chipset and with transceiver 335.
>
> Based on this partitioning, a module that meets the requirements for LMA would contain both transceiver 335 and short range wireless baseband controller 330 of FIG. 1a.

Kardach Application, page 2, column 2, lines 23 – 36. Applicant respectfully requests that the Examiner identify with particularity where in this portion of the Kardach application, or any other portion of the same application, there is disclosed the coupling of the output of a "circuit for controlling the duty cycle and jitter of a clock signal" to the "baseband circuitry of a wireless communications terminal." Applicant respectfully suggests that there is no suggestion in this portion, or any other portion, of the Kardach application, to combine the teaching of the Kardach application with the Kent patent. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claim 3.

For similar reasons as set forth with respect to claim 3, Applicant submits that claim 7 is patentable and respectfully requests the Examiner to withdraw the rejection of claim 7.

E. Rejection of Claims 2 and 6 under 35 U.S.C. § 103(a) as being unpatentable over the Copley Patent in view of the Lee IEEE Reference

Applicant respectfully submits that claims 2 and 6, which respectively depend from claims 1 and 5, are patentable for the same reasons as set forth herein with respect to claims 1 and 5.

In addition, Applicant respectfully submits that the combination of the Copley patent and the Lee IEEE reference neither describes nor suggests "a circuit for controlling the duty cycle and jitter of a clock signal, comprising: an input node for receiving the clock signal; and an output node for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle" where the "predetermined duty cycle is a nominally 50-50 duty cycle" as recited in claim 2.

For these reasons, Applicant respectfully submits that claim 2 is patentable, and therefore requests that the rejection be withdrawn. Applicant also submits that claim 6 is patentable for similar reasons, and requests that the rejection of claim 6 be likewise withdrawn.

F. Rejection of Claims 3 and 7 under 35 U.S.C. § 103(a) as being unpatentable over the Copley Patent in view of the Kardach Application

Applicant respectfully submits that claims 3 and 7 are patentable over the combination of the Copley patent and the Kardach application for reasons similar to those

set forth with respect to the rejection based on the Kardach application in combination with the Kent patent. For example, applicant respectfully requests that the Examiner identify with particularity where in the relied-upon portion of the Kardach application, or any other portion of the same application, there is disclosed the coupling of the output of a "circuit for controlling the duty cycle and jitter of a clock signal" to the "baseband circuitry of a wireless communications terminal." Applicant respectfully submits that no such subject matter is described or suggested in the Kardach application, or in the combination of the Kardach application and the Copley patent, and therefore requests that the Examiner withdraw the rejection of claims 3 and 7 based on this combination.

IV. Conclusion

The Applicant submits that in light of the foregoing remarks the application is now in condition for allowance. Applicant therefore respectfully requests that the outstanding rejections be withdrawn and that the case be passed to issuance.

Respectfully submitted,

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